13.8 An Integrated VCSEL Driver for 10Gb Ethernet in 0.13µm CMOS

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The rapid growth in the deployment of 10Gb/s Ethernet switches for the enterprise market has created a need for low-cost short-reach optical modules in small form-factors such as XENPAK, X2, and XPAK. Recent advances in manufacturing have introduced the vertical cavity surface emitting laser (VCSEL) as a low-power and low-cost alternative to distributed feedback (DFB) and Fabry-Perot (FP) lasers for short-reach applications. A key element in further cost reduction for these optical modules is the integration of a low-power VCSEL driver circuit with the physical layer IC. In this paper, a VCSEL driver implemented with a 10Gb/s Ethernet transceiver [1] in a 0.13µm CMOS process running from a 1.2V supply and dissipating a maximum of 85mW, is presented.

While the drive requirements for a VCSEL are relaxed compared to those for DFB and FP lasers [2, 3], there are unique hurdles in the design of these circuits. First, attaining adequate drive current in a scaled CMOS process operating from a 1.2V supply is challenging. Figure 13.8.1 illustrates single-ended and differential VCSEL configurations. While the tail currents are the same in both cases, the voltage excursion is half as much in the differential case as in the single-ended case, making differential drive the preferred method. However, since the impedance of the VCSEL is typically close to 50Ω, a 25Ω driver is needed for proper impedance matching in this case. Yet, for flexibility in testing and to be able to use the part in 50Ω applications, it is desirable to have a 50Ω driver. Alternatives for meeting both requirements are discussed below. Second, the optical output power of a VCSEL is a strong function of temperature. In order to maintain constant optical power, the modulation current must vary with the laser temperature during normal operation. Precautions for ensuring robust data flow are also discussed in this paper.

Figure 13.8.2 shows two alternatives for implementing the driver circuit. Alternative (a) is an output driver with 50Ω loads, 50Ω transmission lines modeling the package and board traces, 50Ω pullup resistors that match the impedance of the driver to that of the VCSEL, 25Ω transmission lines to the VCSEL, and finally the VCSEL itself. This configuration presents a good impedance match from the VCSEL looking back into the driver. However, it presents an impedance discontinuity from the driver looking towards the VCSEL at the matching resistors. If the driver impedance is well controlled and the lengths of the 50Ω transmission lines are short, the impact of reflections on the eye opening can be minimized.

Alternative (b) uses two 50Ω output drivers in parallel. They connect to 50Ω transmission lines that model the package and board traces, then they short together on the board and drive 25Ω transmission lines into the VCSEL. While the drivers see an impedance mismatch at the shorting point, the transmitted and reflected waves cancel as long as the drivers generate identical waveforms. Therefore, a power combiner is not necessary in this application. Any mismatch in the amplitudes generated by the two drivers causes reflections proportional to the difference in the amplitudes. Mismatch in the delay between the two paths also causes reflections and slows the edge rate of the output by the amount of delay mismatch. Careful IC, package, and board layout can reduce the systematic amplitude and delay mismatch to less than 4% and 2ps, respectively. Random delay mismatch due to variations in the IC- and board-fabrication processes has been estimated at less than 3ps. Therefore, the dual-path approach can be implemented without a significant degradation in performance. This design uses alternative (b) because of its superior signal integrity. The implementation of the driver circuit uses a 4-stage chain of buffers with a fanup ratio of 2. The final driver stage uses inductive peaking to extend the bandwidth and improve the high-frequency impedance matching at the output.

Another consideration is implementing the control loops that keep the optical output power constant as the VCSEL temperature changes. As shown in Fig. 13.8.3, a DOM device is typically mounted near the laser and controls both the dc bias current and the modulation current via two separate loops. It adjusts the dc bias by monitoring an optical power detector and feeding back a control signal to the current source. The DOM also generates temperature readings that the driver circuit uses to index a lookup table containing modulation current values. The control range in the tail current sources is 0 to 18.9mA, in 100µA steps. Since the modulation control loop runs while data is flowing through the transmitter, the DACs that act as the tail current sources must have very low glitch energy to avoid corrupting the data. Therefore, a fully segmented DAC topology is chosen and an FSM is used to change the DAC code in only 1 LSB steps per clock cycle. Since the DAC clock rate is 1MHz and the thermal time constant on the VSCEL die is on the order of 10kHz, loop stability is not compromised.

The output drivers are characterized individually while driving a PRBS pattern of 2^{31}-1 with 16mA tail current. The amplitudes are 662mV and 650mV differential peak-to-peak, and the rise times are 30.2ps and 28.7ps. The combined electrical eye diagram in Fig. 13.8.4 shows only a nominal degradation in the eye relative to the uncombined one. This demonstrates that the requisite matching between the two paths is achieved in this design. Figure 13.8.5 illustrates an optical eye diagram from a VCSEL driven by the integrated VCSEL driver. The rise and fall times are 44ps, which is significantly slower than those for the electrical eye. This is due to the bandlimited response of the VCSEL and will improve as 10Gb/s VCSEL technology continues to mature. Nevertheless, the optical eye exhibits a 35% margin relative to the Ethernet mask. To test the robustness of data transmission while the control loop is operational, the tail currents are swept with a triangular waveform from 4mA to 18.9mA in 100µA steps at the rate of 1µs per step. A 2^{31}-1 PRBS pattern ran error free for three days. A die micrograph is shown in Fig. 13.8.7, and a summary of the VCSEL driver performance is given in Figure 13.8.6.

Acknowledgments:
The authors thank N. Gamini for his packaging expertise, N. Acharya and D. Liu for insightful discussions, B. Cunnie for being a rock-star, and M. Speers for layout support.

References:
[1] S. Sidiropoulos, *et al.*, "An 800mW 10-Gigabit Ethernet Transceiver in 0.13µm CMOS," *ISSCC Dig. Tech. Papers*, pp. 168-169, Feb., 2004.
[2] S. Morley, "A 3V 10.7Gb/s Differential Laser Diode Driver with Active Back Termination Output Stage," *ISSCC Dig. Tech. Papers*, pp. 220-221, Feb., 2005.
[3] S. Galal and B. Razavi, "10-Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18–µm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 38, pp. 2138-2146, Dec., 2003.

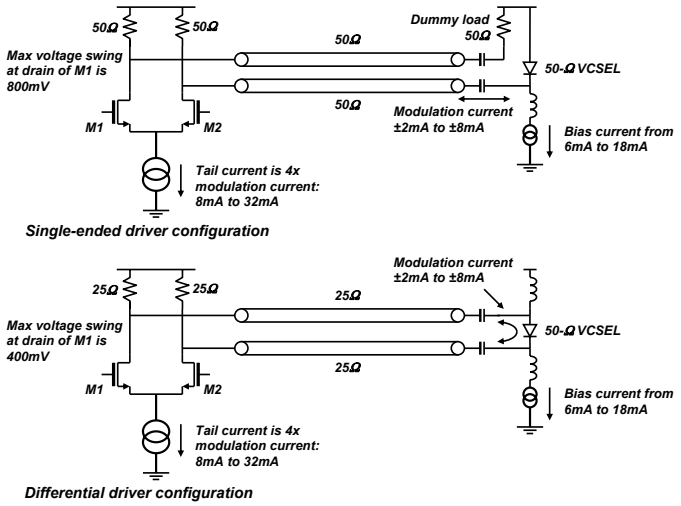

Figure 13.8.1: Single-ended and differential drivers achieving identical current levels in VCSEL.

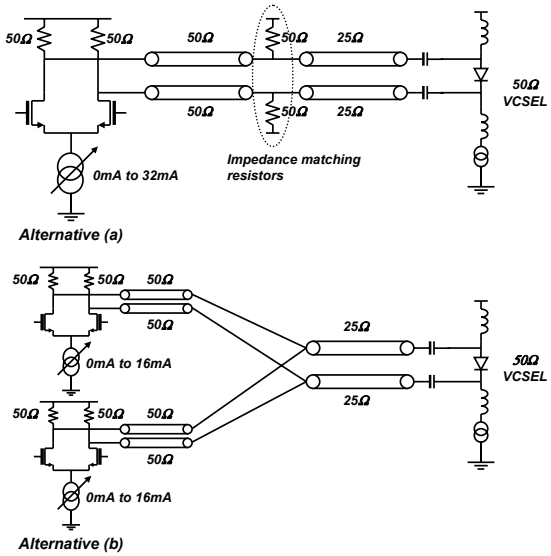

Figure 13.8.2: Two possible implementations for the differential VCSEL driver.

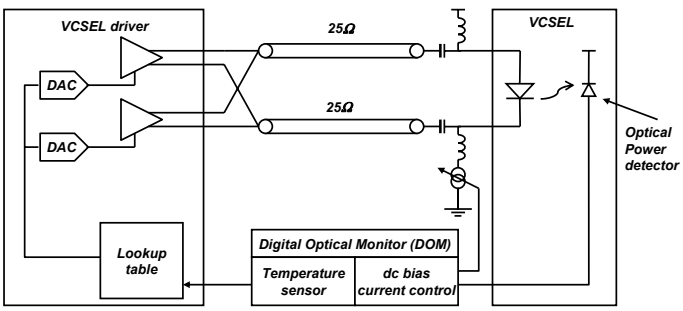

Figure 13.8.3: Optical power control.

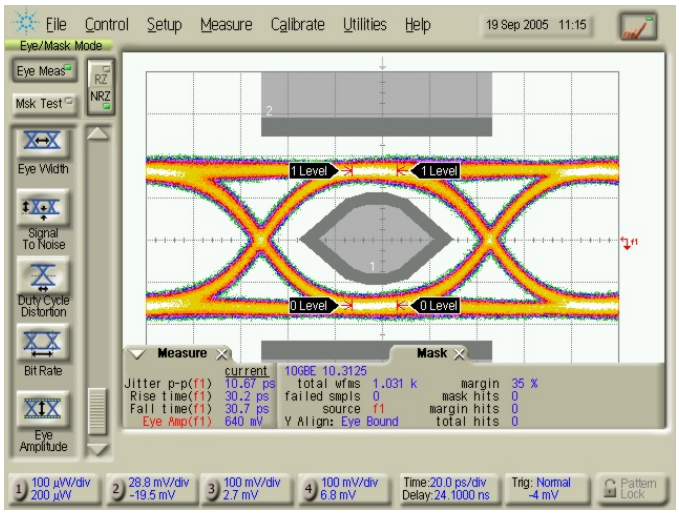

Figure 13.8.4: Electrical eye diagram from combined outputs.

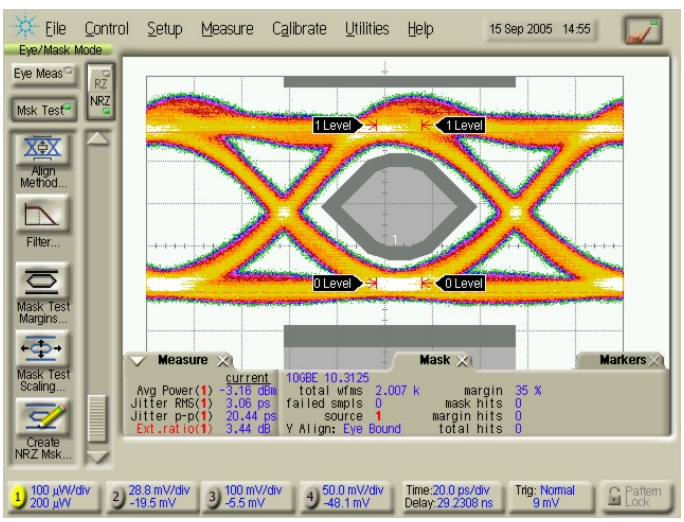

Figure 13.8.5: Optical eye diagram.

Data rate	10.3125Gb/s
Supply voltage	1.2V
Supply current, each path in max current setting	35mA
Die area	0.15µm²
Technology	0.13µm generic CMOS
Modulation current range	±2mA – ±8mA
Rise/fall time, electrical combined	30.2ps
Deterministic jitter, electrical combined	$10.3ps_{pp}$
Random jitter, electrical combined	$2ps_{pp}$
Output swing, electrical combined	$664mV_{,ppd}$

Figure 13.8.6: Performance summary.

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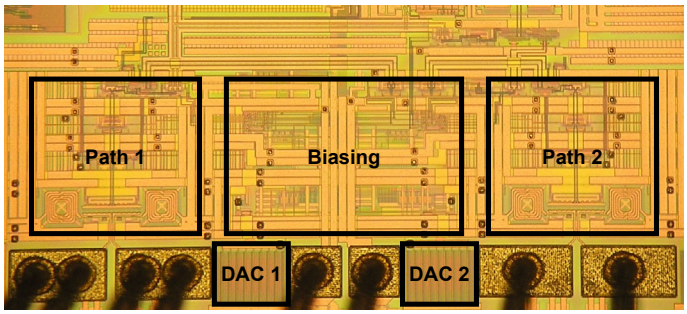

Figure 13.8.7: Die mircograph.

